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the cache a key corresponding to the source address, and using the key to decrypt the body of the packet;

when the source address is not included in an entry of the cache, determining whether the source address is included in an entry of the system memory; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, extracting from the entry of the system memory a key corresponding to the source address, and storing the source address and the key as a new entry in the cache to prepare the cache within the latency period for decrypting a the packet subsequently re-sent by the external source.

14. (Original) A method of key caching as claimed in claim 13, further comprising:

when the source address is not included in an entry of the cache, dropping the packet.

15. (Previously presented) A method of key caching as claimed in claim 13, further comprising:

when the source address is not included in an entry of the cache, authorizing an acknowledgment signal for anticipatory transmission to the external

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source of the packet prior to retrieval of the key corresponding to the source address; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, using the key to decrypt the body of the packet prior to arrival of a subsequent packet from the external source.

16. (Original) A method of key caching as claimed in claim 13, wherein the cache includes fast memory.

17. (Original) A method of key caching as claimed in claim 14, wherein the cache includes fast memory.

18. (Original) A method of key caching as claimed in claim 15, wherein the cache includes fast memory.